What is claimed is:

1. A method for manufacturing a BiCMOS including a bipolar transistor formed of a collector, a base, and an emitter, and a CMOS transistor formed of a gate and a source/drain, the method comprising:

epitaxially growing a SiGe base layer on a substrate;

forming an insulating layer on the SiGe base layer;

forming an emitter window by etching the insulating layer to a partial depth;

forming a dummy polysilicon pattern in the emitter window to have the same height as the surface of the insulating layer;

exposing the sidewalls of the dummy polysilicon pattern and forming dummy spacers on the sidewalls of the dummy polysilicon pattern;

forming an extrinsic base by implanting impurity ions into the SiGe base layer using the dummy polysilicon pattern and the dummy spacers as an ion implantation mask;

removing the dummy spacers and the dummy polysilicon pattern and forming a selective ion-implanted collector in the substrate by implanting impurity ions into the emitter window using the remaining insulating layer as an ion implantation mask;

exposing the SiGe base layer by etching the remaining insulating layer and forming an emitter by depositing and patterning an emitter polysilicon; and

forming a gate and a source/drain.

2. The method of claim 1, wherein forming the SiGe base layer comprises forming an undoped Si layer as a seed layer and sequentially forming a SiGe layer and a doped SiGe layer on the seed layer.

3. The method of claim 1, wherein the insulating layer is formed by depositing several layers, and the top surface of the insulating layer is planarized using chemical mechanical polishing.

4. The method of claim 1, wherein forming the dummy polysilicon pattern comprises:

forming a polysilicon layer on the insulating layer so as to completely fill the emitter window; and

planarizing the polysilicon layer using chemical mechanical polishing until the surface of the insulating layer is exposed and the polysilicon layer remains only in the emitter window.

5. A method for manufacturing a BiCMOS including a first region where a bipolar transistor, which is formed of a collector, a base, and an emitter, will be formed, and a second region where a CMOS transistor, which is formed of a gate and a source/drain, will be formed, the method comprising:

(a) sequentially forming a gate oxide layer and a gate protection polysilicon layer on the first region and the second region;

(b) etching the gate protection polysilicon layer and the gate oxide layer at a portion where the emitter will be formed, in the first region, until a substrate is exposed, and epitaxially growing a SiGe base layer on the exposed substrate;

(c) alternately depositing insulating layers which have an etch selectivity with respect to each other, on the SiGe base layer, sequentially forming a polysilicon layer and an oxide layer, and planarizing the surface of the oxide layer;

(d) forming an emitter window by etching the oxide layer, the polysilicon layer, and parts of the insulating layers in the first region, and forming a dummy polysilicon pattern in the emitter window;

(e) removing the oxide layer and forming dummy spacers on the sidewalls of the dummy polysilicon pattern;

(f) forming an extrinsic base in the SiGe base layer by implanting impurity ions using the dummy polysilicon pattern and the dummy spacers as an ion implantation mask;

(g) removing the dummy spacers, the dummy polysilicon pattern, and the polysilicon layer, and forming a selective ion-implanted collector in the substrate by implanting impurity ions using the insulating layers as an ion implantation mask;

(h) etching the insulating layers remaining in the emitter window and forming an emitter by depositing and patterning an emitter polysilicon;

(i) completing a base by patterning the SiGe base layer in the first region and, at the same time, forming a gate by patterning the SiGe base layer and the gate protection polysilicon in the second region; and

(j) forming spacers on the sidewalls of the emitter, the base, and the gate and forming a source/drain in the second region by implanting impurity ions.

6. The method of claim 5, before step (a) is performed, further comprising:

forming a buried collector layer by implanting impurity ions into the first region of the substrate;

epitaxially growing a collector layer on the buried collector layer;

forming a device isolation layer on a portion of the collector layer excluding an active region; and

forming a sub-collector contact in the first region.

7. The method of claim 5, wherein forming the SiGe base layer comprises forming an undoped Si layer as a seed layer and sequentially forming a SiGe layer and a doped SiGe layer on the seed layer.

8. The method of claim 5, wherein in step (c), the oxide layer is formed using plasma-enhanced chemical vapor deposition and planarized using chemical mechanical polishing.

9. The method of claim 5, wherein forming the dummy polysilicon pattern comprises:

forming a polysilicon layer on the oxide layer to completely fill the emitter window; and

planarizing the polysilicon layer until the top surface of the oxide layer is exposed and the polysilicon layer remains only in the emitter window.

10. The method of claim 5, wherein in step (c), the insulating layers are formed by stacking a first oxide layer, a nitride layer, and a second oxide layer on the SiGe base layer.

11. The method of claim 10, wherein in step (d), the emitter window is formed by etching only the second oxide layer of the insulating layers.

12. The method of claim 11, wherein in step (g), the selective ion-implanted collector is formed after the nitride layer exposed in the emitter window is etched using the etched second oxide layer as an etch mask.

13. The method of claim 5, after step (j) is performed, further comprising forming an ohmic contact including silicide by depositing a metal on the substrate.

14. A method for manufacturing a BiCMOS including a first region where a bipolar transistor, which is formed of a collector, a base, and an emitter, will be formed, and a second region where a CMOS transistor, which is formed of a gate and a source/drain, will be formed, the method comprising:

(a) sequentially forming a gate oxide layer and a gate protection polysilicon layer on the first region and the second region;

(b) exposing a substrate by etching the gate protection polysilicon layer and the gate oxide layer at a portion where the emitter will be formed, in the first region, and epitaxially growing a SiGe base layer;

(c) sequentially forming a first oxide layer, a nitride layer, a second oxide layer, a polysilicon layer, and a third oxide layer on the SiGe base layer and planarizing the surface of the third oxide layer;

(d) opening an emitter window by etching the third oxide layer, the polysilicon layer, and the second oxide layer in the first region, and forming a dummy polysilicon pattern in the emitter window to have the same height as the surface of the third oxide layer;

(e) removing the third oxide layer and forming dummy spacers on the sidewalls of the dummy polysilicon pattern;

(f) forming an extrinsic base by implanting impurity ions into the SiGe base layer using the dummy polysilicon pattern and the dummy spacers as an ion implantation mask;

(g) removing the dummy spacers, the dummy polysilicon pattern, and the polysilicon layer, etching the nitride layer using the etched second oxide layer as an etch mask, and forming a selective ion-implanted collector by implanting impurity ions into the emitter window using the second oxide layer and the nitride layer as an ion implantation mask;

(h) etching the second oxide layer and the first oxide layer remaining in the emitter window, depositing an emitter polysilicon on the SiGe base layer, and forming an emitter by patterning the emitter polysilicon and the nitride layer;

(i) completing a base by patterning the SiGe base layer and the gate protection polysilicon layer in the first region and, at the same time, forming a gate by patterning the SiGe base layer and the gate protection polysilicon layer; and

(j) forming spacers on the sidewalls of the emitter, the base, and the gate and forming a source/drain in the second region by implanting impurity ions.

15. The method of claim 14, before step (a) is performed, further comprising:

forming a buried collector layer by implanting impurity ions into the first region of the substrate;

epitaxially growing a collector layer on the buried collector layer;

forming a device isolation layer on the collector layer excluding an active region; and

forming a sub-collector contact in the first region.

16. The method of claim 14, wherein forming the SiGe base layer comprises forming an undoped Si layer as a seed layer and sequentially forming a SiGe layer and a doped SiGe layer on the seed layer.

17. The method of claim 14, wherein in step (c), the third oxide layer is formed using plasma-enhanced chemical vapor deposition and planarized using chemical mechanical polishing.

18. The method of claim 14, wherein forming the dummy polysilicon pattern comprises:

forming a polysilicon layer on the third oxide layer to completely fill the emitter window; and

planarizing the polysilicon layer until the top surface of the third oxide layer is exposed and the polysilicon layer remains only in the emitter window.

19. The method of claim 14, after step (j) is performed, further comprising forming an ohmic contact including silicide by depositing a metal on the substrate.